What is claimed is:

1. A method of fabricating a semiconductor device, comprising:

forming a MOS transistor at a predetermined region of a semiconductor substrate, the MOS transistor being formed to have a source region and a drain region spaced apart from each other as well as a gate electrode located over a channel region between the source and drain regions;

forming a stress layer on the semiconductor substrate having the MOS transistor; and

annealing the stress layer to convert a physical stress of the stress layer into a tensile stress or increase a tensile stress of the stress layer.

2. The method according to claim 1, wherein the MOS transistor is an NMOS transistor.

3. The method according to claim 1, further comprising forming a nickel silicide layer on the gate electrode and/or the source and drain regions using a salicide technique prior to formation of the stress layer.

4. The method according to claim 1, wherein the stress layer is formed of an insulating layer having a tensile stress.

5. The method according to claim 4, wherein the insulating layer having the tensile stress is formed of at least one layer selected from the group consisting of a silicon nitride layer, a silicon oxynitride layer, an LPCVD oxide layer, an ALD oxide layer and an SOG layer.

6. The method according to claim 5, wherein the silicon nitride layer and the silicon oxynitride layer are formed using a plasma CVD technique or an ALD technique at a temperature below 500℃.

7. The method according to claim 1, wherein the stress layer is formed to a thickenss of 50-2000Å.

8. The method according to claim 1, wherein annealing the stress layer is performed at a temperature of 400-550Å.

9. The method according to claim 8, wherein annealing the stress layer is performed using a nitrogen gas as an ambient gas.

10. A method of fabricating a semiconductor device, comprising:

forming an isolation layer at a predetermined region of a semiconductor substrate to define an active region;

forming a gate electrode crossing over the active region;

forming spacers on sidewalls of the gate electrode;

implanting N-type impurity ions into the active region using the gate electrode and the spacers as ion implantation masks to form an N-type source region and an N-type drain region at both sides of the gate electrode;

forming a nickel silicide layer on the gate electrode and the source and drain regions using a salicide technique;

forming a stress layer on the semiconductor substrate including the nickel silicide layer;

annealing the stress layer to convert a physical stress of the stress layer into a tensile stress or increase a tensile stress of the stress layer; and

forming an interlayer insulating layer on the annealed stress layer.

11. The method according to claim 10, further comprising implanting N-type impurity ions into the active region using the gate electrode and the isolation layer as ion implantation masks to form N-type LDD regions prior to formation of the spacers.

12. The method according to claim 10, wherein the nickel silicide layer is a pure nickel silicide layer or a nickel alloy silicide layer.

13. The method according to claim 12, wherein the nickel alloy silicide layer contains at least one material selected from the group consisting of tantalum

(Ta), zirconium (Zr), titanium (Ti), hafnium (Hf), tungsten (W), cobalt (Co), platinum (Pt), molybdenum (Mo), palladium (Pd), vanadium (V) and niobium (Nb).

14. The method according to claim 10, wherein the stress layer is formed of at least one layer selected from the group consisting of a silicon nitride layer, a silicon oxynitride layer, an LPCVD oxide layer, an ALD oxide layer and an SOG layer.

15. The method according to claim 14, wherein the silicon nitride layer and the silicon oxynitride layer are formed at a temperature below 500℃ using a plasma CVD technique or an ALD technique.

16. The method according to claim 10, wherein the stress layer is formed to a thickness of 50-2000Å.

17. The method according to claim 10, wherein annealing the stress layer is performed at a temperature of 400-550℃.

18. The method according to claim 17, wherein annealing the stress layer is performed using a nitrogen gas as an ambient gas.

19. A method of fabricating a semiconductor device, comprising:

forming an isolation layer at a predetermined region of a semiconductor substrate to define an active region;

forming a gate electrode crossing over the active region;

forming spacers on sidewalls of the gate electrode;

implanting N-type impurity ions into the active region using the gate electrode and the spacers as ion implantation masks to form an N-type source region and an N-type drain region at both sides of the gate electrode;

forming a nickel silicide layer on the gate electrode and the source/drain regions using a salicide technique;

forming a stress layer on the semiconductor substrate including the nickel silicide layer;

forming a lower interlayer insulating layer on the stress layer;

patterning the lower interlayer insulating layer to selectively expose the stress layer over the active region;

annealing the exposed stress layer to convert a physical stress of the exposed stress layer into a tensile stress or increase a tensile stress of the exposed stress layer; and

forming an upper interlayer insulating layer on the semiconductor substrate having the annealed stress layer.

20. The method according to claim 19, further comprising implanting N-type ions into the active region using the isolation layer and the gate electrode as

ion implantation masks to form N-type LDD regions at both sides of the gate electrode, prior to formation of the spacers.

21. The method according to claim 19, wherein the nickel silicide layer is a pure nickel silicide layer or a nickel alloy silicide layer.

22. The method according to claim 21, wherein the nickel alloy silicide layer contains at least one material selected from the group consisting of tantalum (Ta), zirconium (Zr), titanium (Ti), hafnium (Hf), tungsten (W), cobalt (Co), platinum (Pt), molybdenum (Mo), palladium (Pd), vanadium (V) and niobium (Nb).

23. The method according to claim 19, wherein the stress layer is formed of at least one layer selected from the group consisting of a silicon nitride layer, a silicon oxynitride layer, an LPCVD oxide layer, an ALD oxide layer and an SOG layer.

24. The method according to claim 23, wherein the silicon nitride layer and the silicon oxynitride layer are formed at a temperature below 500℃ using a plasma CVD technique or an ALD technique.

25. The method according to claim 19, wherein the stress layer is formed to a thickness of 50-2000Å.

26. The method according to claim 19, wherein annealing the exposed stress layer is performed at a temperature of 400-550℃.

27. The method according to claim 26, wherein annealing the stress layer is performed using a nitrogen gas as an ambient gas.